Laboratory #1
Multi-Stage Amplifiers

I. Objectives

1. Learn the basic knowledge of cascode and cascade amplifier
2. Comparison of the characteristics of CS (common-source) amplifier and CS-CG cascode amplifier

II. Components and Instruments

1. Components
   (1) MOSFET array IC: CD4007 ×1
   (2) Resistor: 1MΩ ×1
   (3) Variable Resistor: 1MΩ ×1, 10kΩ ×1
   (4) Capacitor: 0.1μF ×1
2. Instruments
   (1) DC power supply (Keysight E36311A)
   (2) Digital multimeter (Keysight 34450A)
   (3) Oscilloscope (Agilent MSOX 2014A)

III. Reading

1. Section 6-3 to 6-13 and 8.1-8.9 of "Microelectronics Circuits 6th edition, Sedra/Smith".

IV. Preparation

1. Introduction
   (1) The MOSFET cascode configuration
   (2) CS-CG cascode amplifier
   (3) CS-CD cascade amplifier

In Microelectronics and Circuitry Laboratory(I) Lab.12, the characteristics of single stage MOS amplifiers had been introduced and verified. In this Lab. 1, their cascode and cascade configurations will be presented. These configurations are commonly used for some specific purposes, such as high gain or wide bandwidth applications. Cascode configuration can increase the dc gain of the amplifier through the increasing of the output impedance. For example, multistage CMOS amplifier can increase its gain by cascoding CS (common source) amplifier and CG (common gate) amplifier. Other than that, another important performance index of

OPAMP is its bandwidth, where wider bandwidth OPAMP can be applied for high speed applications. Therefore, by applying Miller theorem to the CS amplifier with cascading the CD (common drain) amplifier, the bandwidth can significantly be extended. Furthermore, the analysis of the differential amplifier can also be started from CD-CG (common gate) configuration.

In Lab. 1, we take CS-CG configuration as an example for experiment of the multistage CMOS amplifier. Part 2 will briefly illustrate the MOSFET cascode configuration and compared with the single stage configuration. Following that, CD-CS and CD-CG configuration will be introduced in Part 3 and Part 4 respectively.

2. The MOSFET cascode configuration

The schematic of the cascode amplifier is shown as below:

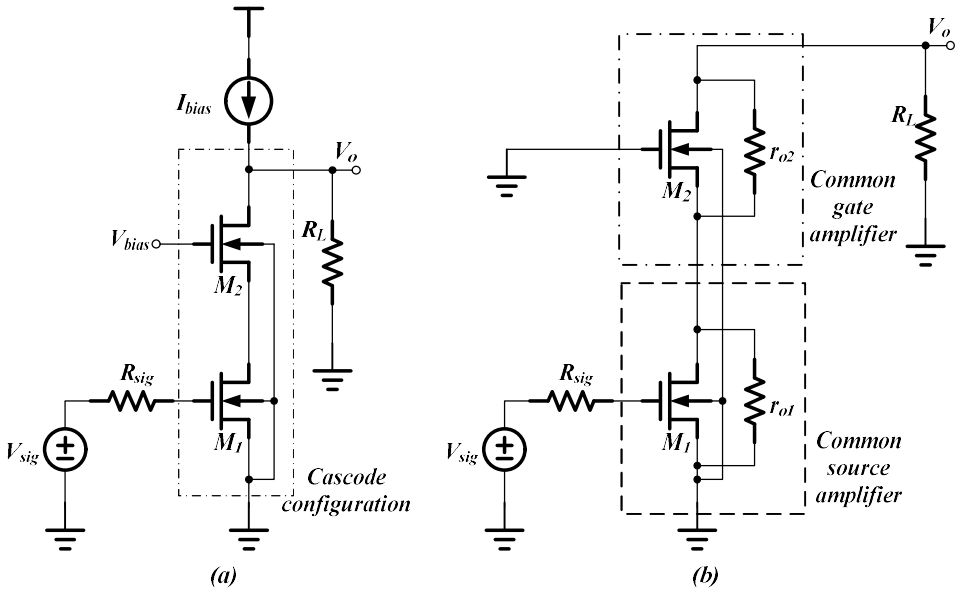

Fig. 1.1 (a) Schematic of the MOSFET cascode configuration
(b) DC analytical model of the cascode configuration

Fig.1.1 (a) shows the circuit diagram of the cascode amplifier, this configuration often used for increasing the output impedance of an amplifier. The DC analytical model is shown in Fig.1.1 (b), the DC gain can easily be derived as the order of $g_m r_o^2$, where the transconductance g_m is determined by the current source I_{bias} as shown in Fig.1.1 (a). Note that the high output impedance of the cascode configuration is targeted at high gain, but the load resistance must be comparable with the output impedance, or the DC gain will be limited by the load resistance. With the DC analysis described above, the AC analysis can further be performed in Fig.1.2.

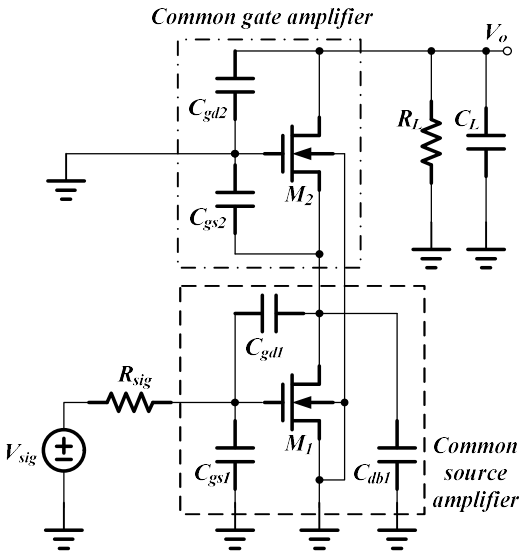

Fig. 1.2 AC analytical model of the MOSFET cascode configuration

Fig. 1.2 shows the basic cascode configuration, the parasitic capacitance is shown in this schematic for analyzing its high-frequency model. With the analysis of the cascode configuration, the characteristics of the cascode can be figured out.

The analysis of the frequency response can be started from open-circuit-time-constants method, which is commonly performed in linear circuit modeling. The dominant pole can be analyzed from the sum of the time constants seen from the following four capacitances; C_{gs1}, C_{gd1}, $C_{db1}+C_{gs2}$, and C_L+C_{gd2}.

a. The impedance seen from C_{gs1} is R_{sig}.
b. By adopting Miller theorem, R_{gd1} can be derived as $R_{gd1}=(1+g_{m1}R_{d1})R_{sig}+R_{d1}$.
c. The impedance seen from $C_{db1}+C_{gs2}$ is R_{d1}.
d. The output impedance paralleled with the load resistance will be the total impedance seen from C_L+C_{gd2}.

Hence, the effective time constant τ_H can be calculated as

$$\tau_H= R_{sig}\,[C_{gs1}+ C_{gd1}(1+g_{m1}R_{d1})]+ R_{d1}(C_{gd1}+ C_{db1}+C_{gs2})+(R_L||R_{out})(C_L+C_{gd2})$$

In the case of small R_{sig}, the Miller effect at M1 will not be of concern. Also, the second term will be smaller than the third term, thus the effective time constant can be rewritten as

$$\tau_H= (R_L||R_{out})(C_L+C_{gd2})$$

And the 3-dB frequency becomes

$$f_H= 1/2\,\pi\,(R_L||R_{out})(C_L+C_{gd2})$$

Now consider that as load resistance is close to the order of the output impedance, the comparisons of the characteristics of cascode amplifier and CS amplifier can be listed as Table 1.1. And the comparison of the frequency response is shown in Fig. 1.3.

Table 1.1 Comparison of the characteristics of CS and cascode amplifier

	Common Source	Cascode
DC gain	$-g_mR_L'$	$-g_m^2r_oR_L'$
f_{3dB}	$1/2\pi(R_L\|\|R_{out})(C_L+C_{gd})$	$1/2\pi g_mr_o(R_L\|\|R_{out})(C_L+C_{gd})$
f_t	$g_m/2\pi(C_L+C_{gd})$	$g_m/2\pi(C_L+C_{gd})$

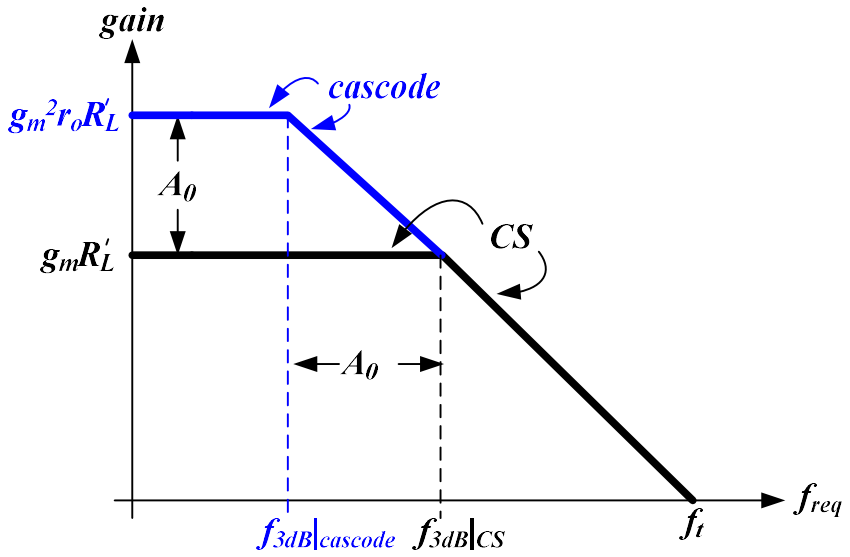

Fig. 1.3 Comparison of the frequency response

3. CD-CS cascade amplifier

Part 2 has briefly introduced a common technique for obtaining larger DC gain compared with the CS single-stage amplifier. There is also a common solution for extending the bandwidth of an amplifier, which is CD-CS cascade amplifier as shown in Fig. 1.4.

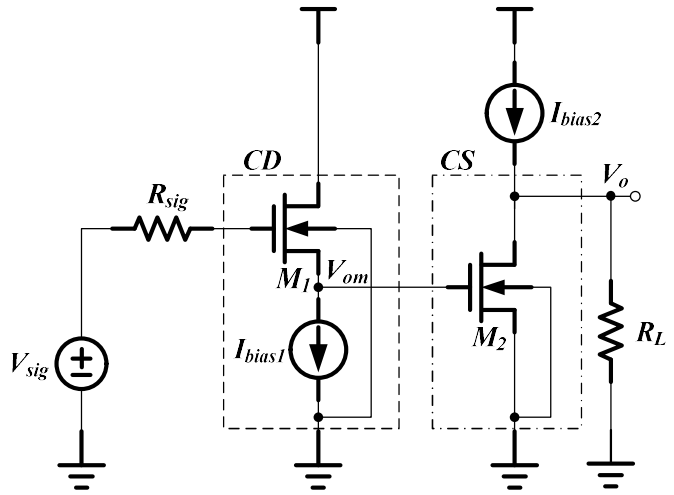

Fig. 1.4 CD-CS cascade configuration

DC gain of the cascade amplifier will be slightly lower compared with the CS amplifier. Its high-frequency model can also be derived with the open-circuit-time-constant method as described previously. The equivalent input resistance of such configuration is greatly reduced by $g_m r_o$ when compared with CS amplifier. Hence the effective time constant is significantly reduced and the bandwidth can is extended.

4. CD-CG amplifier

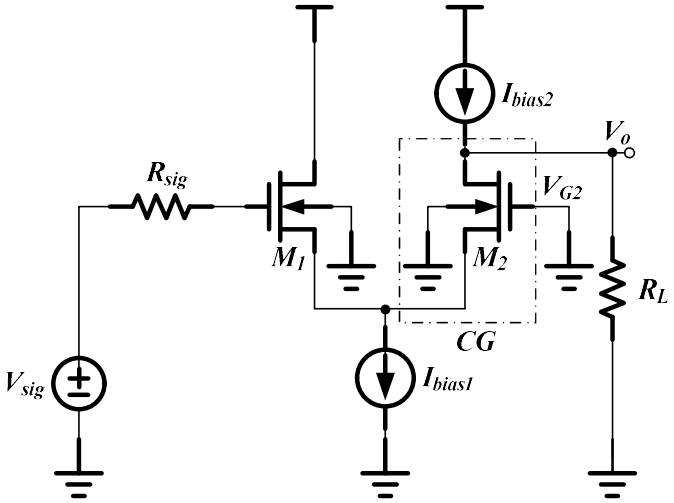

Fig. 1.5 CD-CG cascade configuration

The analysis of the differential amplifier can be thought as the superposition of the M1-M2 pair (CD-CG) and M2 (CS amplifier). Hence the gain of the differential amplifier can be derived as $g_m r_o$.

V. Exploration

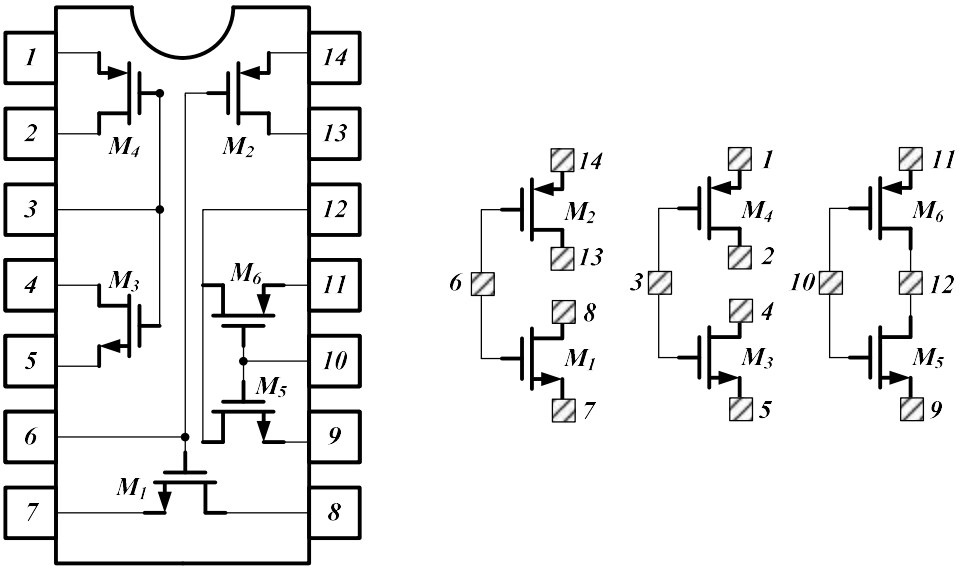

Fig. 1.6 Pin diagram of CD4007

1. Explore the small signal model of CS and CS-CG amplifier

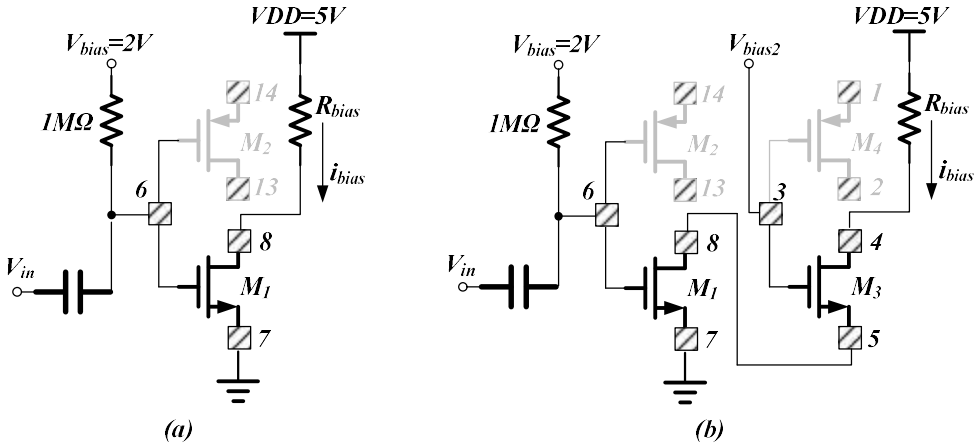

Fig. 1.7 Setup of the (a) CS and (b) CS-CG amplifier

(1) Design the CS amplifier to be operated with about 15dB~20dB DC gain with coupling capacitor = 0.1μF, R_{bias} = 1MΩ variable resistor. Recording the bias current I_{bias}. Record the DC gain of this CS-CG amplifier in Table 1.3.

(2) Adjust the bias voltage V_{bias2}, when the same resistance R_{bias} is used and the M1 and M3 are biased at the current as (1). Record the DC gain of this CS-CG amplifier in Table 1.4.

2. Complete the bode plot of both CS and CS-CG amplifier as shown in Fig. 1.7 (a) and (b).

Laboratory #1 Pre-lab

Class:

Name: Student ID:

1. Explore the frequency response of CS amplifier,

   (1) Use PSpice to do the ac analysis on the circuit below, and show the plot of frequency response of Vo/Vi (dB). Note that the NMOS model is NMOSOP5_BODY, and PMOS model is PMOSOP5_ BODY, which can be used when Sedra library is included. Schematic of the circuit is shown in Fig. 1.8 and the values of components' parameters are all listed in Table 1.2.

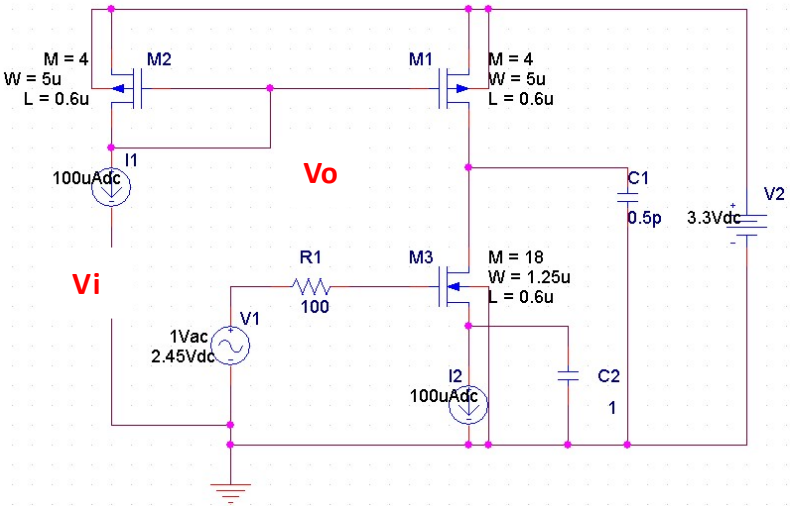

Fig. 1.8 Schematic of the CS amplifier for AC analysis

Table 1.2 Values of components' parameters of the CS amplifier

Component	Spec.	
	W/L (μm)	M
M1	5/0.6	4
M2	5/0.6	4
M3	1.25/0.6	18
R1	100Ω	
C1	0.5pF	
C2	1F	
V1	DC 2.45V with AC 1V	
V2	DC 3.3V	
I1	100μA	
I2	100μA	

2. Explore the frequency response of CS-CG folded-cascode amplifier,

(1) To avoid the problem of limited operating range resulted from transistor stacking in cascode configuration. Folded-cascode is a more common topology in modern circuit design. By folding the PMOS down, DC gain remains the same as cascode configuration, but the input common-mode range has been improved. The circuit is as shown in Fig. 1.9.

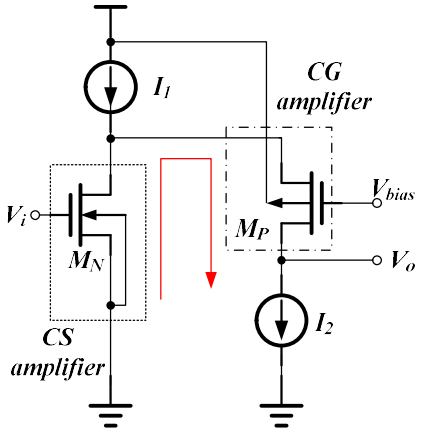

Fig. 1.9 Schematic of the folded-cascode amplifier

Use PSpice to do the ac analysis on the circuit shown in Fig.1.10, and show the plot of frequency response of Vo/Vi (dB)

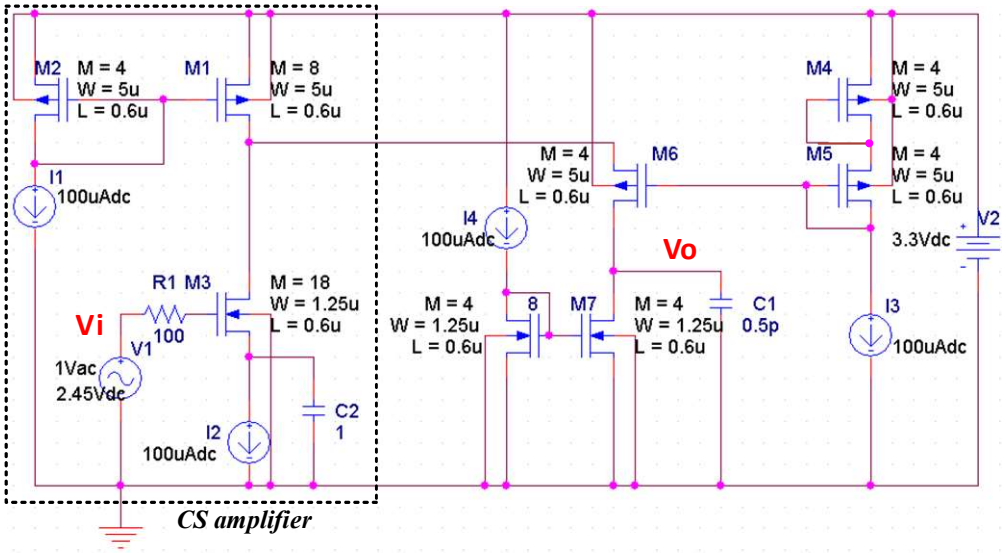

Fig. 1.10 Schematic of the CS-CG cascode amplifier

(2) Which of the transistor is operated as CG configuration, similar to the function of M_P in Fig. 1.9?

Laboratory #1 Report

Class:

Name: Student ID:

1. Exploration 1

   (1) Bias current I_{bias}=_____μA.

   (2) The bias voltage V_{bias2} =_____V

2. Exploration 2

   (1) Experimental result of CS amplifier

Table 1.3

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{o,p-p}$ (mV)	$V_{o,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
50	200		
100	200		
1k	200		
10k	200		
20k	200		
50k	200		
100k	200		
200k	200		
500k	200		
1Meg	200		
1.2Meg	200		
1.5Meg	200		
1.7Meg	200		
2Meg	200		
2.2Meg	200		
2.5Meg	200		

(2) The figure of "($V_{o,p-p}/V_{i,p-p}$) to freq", f_{3dB} = _____Hz; f_t = _____Hz

(3) Experimental result of CS-CG amplifier

(4) The

Table 1.4

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{o,p-p}$ (mV)	$V_{o,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
50	200		
100	200		
1k	200		
10k	200		
20k	200		
50k	200		
100k	200		
200k	200		
500k	200		
1Meg	200		
1.2Meg	200		
1.5Meg	200		
1.7Meg	200		
2Meg	200		
2.2Meg	200		
2.5Meg	200		

figure of "($V_{o,p-p}/V_{i,p-p}$) to freq", f_{3dB} = _____Hz; f_t = _____Hz

3. Problem 1

Compare the voltage waveforms of input to output, what type is the CS-CG multistage amplifier (inverting or non-inverting)? Why?

4. Problem 2

Briefly explain the advantages and disadvantages of CS-CG multistage amplifier.

5. Conclusion